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09/815,781	03/23/2001	Hitoshi Ebihara	SCEI 3.0-041	5299

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EXAMINER	
QUILLEN, ALLEN E	

ART UNIT	PAPER NUMBER
2676	19

DATE MAILED: 02/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/815,781	EBIHARA ET AL.	
	Examiner	Art Unit	
	Allen E. Quillen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 110-140* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 110-140* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Applicant's arguments with respect to claims 1, 110 have been considered but are moot in view of the new ground(s) of rejection. Amended claims 1, 110 emphasize a single display; Claims 1-10, 110-140 are pending.

Election/Restrictions

2. In paper number 11, filed July 16, 2003, Applicant elected Species (a) below, Figures 3-9, Claims 1-11, 110-140.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claim 1-11, 110-140 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiraz, U.S. Patent 6,411,302, Littlefield, U.S. Patent 4,949,280, MacInnis, et al, U.S. Patent 6,573,905, in further view of Bright, et al, U.S. Patent 6,128,025.

5. Regarding claim 1, representative of claims 9, 11, 110, 118, 124, 127, 138, 139, Chiraz discloses an apparatus for processing image data to produce an image for covering an image area of a single display (Figure 1, Column 11, lines 9-14; Figure 23A-B, Column 21, lines 39-60; Column 38, lines 40-46), comprising: a plurality of processors (Figure 9, elements 32A, 32N, Column 13, lines 28-32; Figure 25, elements 176, 180, 184, Columns 23-24; Column 16, lines 54-57; *AGP Bus*, Column 13, lines 36; I, Column 16, lines 54-58), each processor being operable to render the image data into frame image data and to store the frame image data in a respective local frame buffer (Column 13, lines 20-27); a control processor (*CPU*, Column 6, line 30) operable to provide instructions (*graphics commands*, Figure 25; *DirectDraw, lines 51-55; GDI calls*, Column 18, lines 35-38) to the plurality of processors.

[Claim 11 further] Chiraz discloses one of more modes (*full screen, page flipping,* Column 7, lines 23-38).

Chiraz teaches graphics processing (Columns 20-24) using multiple processors and Accelerated Graphics Port (AGP) (Figure 9, Column 13, lines 27-49; Column 3, lines 35), but does not disclose a plurality of graphics processors. Littlefield teaches plurality of graphics processors (Figures 1-8, Column 4, line 60-64). The motivation for combining multiple frame buffers with multiple graphics processors is to allow unrestrained pixel mapping (Column 3, lines 40-49). Littlefield is evidence that at the time of the invention, it would have been obvious to one skilled in designing image processing machines, to combine the benefits of multiple processors and multiple frame buffers, as Chiraz discloses, with multiple graphics processors, as Littlefield teaches, to enable unrestrained pixel mapping.

Chiraz does not disclose and one or more merge units operable to synchronously receive the frame image data; from the respective local frame buffers and to synchronously produce combined frame image data based thereon. MacInnis teaches and one or more merge units operable to synchronously receive the frame image data; from the respective local frame buffers and to synchronously produce combined frame image data based thereon (Column 6, line 17; Figure 4, elements 94, 108; Column 9, lines 25-36). The motivation for combining frame image data processing using multiple frame buffers and multiple displays with one or more merge units is to blend various graphics layers and the appropriate alpha blend values for the video layers to enable a single logical display surface (Column 6, lines 29-30). MacInnis is evidence that at the time of the invention, it would have been obvious to one skilled in the art of logical screen frame-based data processing to combine the benefits of multiple processors and multiple

displays, as Chiraz discloses, with digitized video graphics merge units, as MacInnis teaches, to blend various graphics layers to achieve a single logical screen.

Chiraz does not disclose synchronously produce frame image data. Bright teaches synchronously produce frame image data (Column 2, lines 48-50, 55-58; Column 9, lines 55-60, *each driving a portion of the LCD display*). The motivation for combining combined frame image data processing using multiple frame buffers and multiple displays with synchronous frame image data is to enable the graphics controller (*rendering engine*, Column 1, line 25) to generate row and column addresses for refreshing the display (Column 1, lines 48-60). Bright is evidence that at the time of the invention, it would have been obvious to one skilled in the art of logical screen frame-based data processing to combine the benefits of multiple processors and multiple displays, as Chiraz discloses, with synchronization using timing logic, as Bright teaches, to enable the graphics controller (*rendering engine*, Column 1, line 25) to generate row and column addresses for refreshing the display (Column 1, lines 48-60).

6. Regarding claim 2, representative of claims 3, 10, 117, Chiraz discloses an apparatus of claim 1, wherein the graphics processors release the frame image data from the respective local frame buffers to produce the frame image (see above).

Chiraz does not disclose from the respective local frame buffers at least one of the one or more merge units is operable to produce the frame image. MacInnis teaches and one or more merge units operable to synchronously receive the frame image data (Figure 4, elements 94, 108; Figure 69, elements 2730A-2730C; Column 108, lines 54-65). The motivation for combining frame image data processing using multiple frame buffers and multiple displays with one or

more merge units is to blend various graphics layers and the appropriate alpha blend values for the video layers to enable a single logical display surface (Column 6, lines 29-30). MacInnis is evidence that at the time of the invention, it would have been obvious to one skilled in the art of logical screen frame-based data processing to combine the benefits of multiple processors and multiple displays, as Chiraz discloses, with digitized video graphics merge units, as MacInnis teaches, to blend various graphics layers to achieve a single logical screen.

Chiraz does not disclose a merge synchronization signal used by the graphics processors to release the frame image data from the respective local frame buffers to the one or more merge units. Bright teaches from the respective local frame buffers and to synchronously produce combined frame image data based thereon (Column 2, lines 48-50, 55-58; Column 9, lines 55-60, *each driving a portion of the LCD display*). The motivation for combining frame image data processing using multiple frame buffers and multiple displays with synchronously combined frame image data is to enable the graphics controller (*rendering engine*, Column 1, line 25) to generate row and column addresses for refreshing the display (Column 1, lines 48-60). Bright is evidence that at the time of the invention, it would have been obvious to one skilled in the art of logical screen frame-based data processing to combine the benefits of multiple processors and multiple displays, as Chiraz discloses, with synchronization using timing logic, as Bright teaches, to enable the graphics controller (*rendering engine*, Column 1, line 25) to generate row and column addresses for refreshing the display (Column 1, lines 48-60).

7. Regarding claim 4, representative of claims 5-8, 111-113, Chiraz, MacInnis, Bright discloses an apparatus of claim 2.

Chiraz does not disclose, wherein the merge synchronization signal is synchronized in accordance with a display protocol defining how respective frames of the combined frame image data are to be displayed. Bright teaches from the respective local frame buffers and to synchronously produce combined frame image data based thereon (Column 2, lines 48-50, 55-58; Column 9, lines 55-60, *each driving a portion of the LCD display*). The motivation for combining frame image data processing using multiple frame buffers and multiple displays with synchronously combined frame image data is to enable the graphics controller (*rendering engine*, Column 1, line 25) to generate row and column addresses for refreshing the display (Column 1, lines 48-60). Bright is evidence that at the time of the invention, it would have been obvious to one skilled in the art of logical screen frame-based data processing to combine the benefits of multiple processors and multiple displays, as Chiraz discloses, with synchronization using timing logic, as Bright teaches, to enable the graphics controller (*rendering engine*, Column 1, line 25) to generate row and column addresses for refreshing the display (Column 1, lines 48-60).

8. Regarding claim 119, representative of claims 120-123, 125-126, 128, 130-136, 137, Chiraz discloses a method of claim 110, wherein the graphics processors can operate in one or more modes (*full screen, page flipping,* Column 7, lines 23-38) that affect when image data are rendered, when frame image data produce the image data (column 42, lines 25-46).

Chiraz does not disclose released from the respective local frame buffers when and how frame image data are merged to produce the combined frame image data. MacInnis teaches released from the respective local frame buffers when and how frame image data are merged to produce the combined frame image data (Figure 4, elements 94, 108; Figure 69, elements

2730A-2730C; Column 108, lines 54-65). The motivation for combining frame image data processing using multiple frame buffers and multiple displays with one or more merge units is to blend various graphics layers and the appropriate alpha blend values for the video layers to enable a single logical display surface (Column 6, lines 29-30). MacInnis is evidence that at the time of the invention, it would have been obvious to one skilled in the art of logical screen frame-based data processing to combine the benefits of multiple processors and multiple displays, as Chiraz discloses, with digitized video graphics merge units, as MacInnis teaches, to blend various graphics layers to achieve a single logical screen.

Chiraz does not disclose a merge (i) timing relationships [synchronization signal] used by the graphics processors to (ii) synchronously release the frame image data from the respective local frame buffers to the one or more merge units. Bright teaches from the respective local frame buffers and to synchronously produce combined frame image data based thereon (Column 2, lines 48-50, 55-58; Column 9, lines 55-60, *each driving a portion of the LCD display*). The motivation for combining frame image data processing using multiple frame buffers and multiple displays with synchronously combined frame image data is to enable the graphics controller (*rendering engine*, Column 1, line 25) to generate row and column addresses for refreshing the display (Column 1, lines 48-60). Bright is evidence that at the time of the invention, it would have been obvious to one skilled in the art of logical screen frame-based data processing to combine the benefits of multiple processors and multiple displays, as Chiraz discloses, with synchronization using timing logic, as Bright teaches, to enable the graphics controller (*rendering engine*, Column 1, line 25) to generate row and column addresses for refreshing the display (Column 1, lines 48-60).

9. Regarding claim 124, representative of claim 127, Chiraz discloses the method of claim 122, further comprising the at least two graphics processors (see above).

Chiraz does not disclose aggregating the frame image data from the respective rendering areas of and the combined frame image data are capable of covering the image area. MacInnis teaches released from the respective local frame buffers when and how frame image data are merged to produce the combined frame image data (Figure 4, elements 94, 108; Figure 69, elements 2730A-2730C; Column 108, lines 54-65). The motivation for combining frame image data processing using multiple frame buffers and multiple displays with one or more merge units is to blend various graphics layers and the appropriate alpha blend values for the video layers to enable a single logical display surface (Column 6, lines 29-30). MacInnis is evidence that at the time of the invention, it would have been obvious to one skilled in the art of logical screen frame-based data processing to combine the benefits of multiple processors and multiple displays, as Chiraz discloses, with digitized video graphics merge units, as MacInnis teaches, to blend various graphics layers to achieve a single logical screen.

Chiraz does not disclose based on alpha blending values to produce the combined frame image data. MacInnis teaches based on alpha blending values to produce the combined frame image data (*alpha values, final blended result,* Column 46, lines 1-65). The motivation for combining frame image data processing using multiple frame buffers and multiple displays with alpha blending is for layering and weighted sum averaging of previous alpha values (Column 9, lines 30-36). MacInnis is evidence that at the time of the invention, it would have been obvious to one skilled in the art of logical screen frame-based data processing to combine the benefits of

multiple processors and multiple displays, as Chiraz discloses, with digitized video graphics alpha blending, as MacInnis teaches, to blend various graphics layers to achieve a single logical screen.

Chiraz does not disclose synchronously. Bright teaches from the respective local frame buffers and to synchronously produce combined frame image data based thereon (Column 2, lines 48-50, 55-58; Column 9, lines 55-60, *each driving a portion of the LCD display*). The motivation for combining frame image data processing using multiple frame buffers and multiple displays with synchronously combined frame image data is to enable the graphics controller (*rendering engine*, Column 1, line 25) to generate row and column addresses for refreshing the display (Column 1, lines 48-60). Bright is evidence that at the time of the invention, it would have been obvious to one skilled in the art of logical screen frame-based data processing to combine the benefits of multiple processors and multiple displays, as Chiraz discloses, with synchronization using timing logic, as Bright teaches, to enable the graphics controller (*rendering engine*, Column 1, line 25) to generate row and column addresses for refreshing the display (Column 1, lines 48-60).

10. Regarding claim 129, representative of claim 132, Chiraz discloses a method of claim 128, further comprising frame image data may overwrite another (Column 24, lines 56-61)

Chiraz does not disclose the layers of frame image data depending on the priority of the layers or synchronously layering the frame image data such that one of the layers of frame image data. MacInnis teaches the layers of frame image data depending on the priority of the layers or synchronously layering the frame image data such that one of the layers of frame

image data (Column 46, lines 1-30). The motivation for combining frame image data processing using multiple frame buffers and multiple displays using overwrite with layering is to avoid processing and storing data that is not to be displayed (Column 46, lines 37-51). MacInnis is evidence that at the time of the invention, it would have been obvious to one skilled in the art of logical screen frame-based data processing to combine the benefits of multiple processors and multiple displays using memory overwrite, as Chiraz discloses, with digitized video graphics alpha blending in layers, as MacInnis teaches, to avoid unnecessary processing and storage costs.

11. Regarding claim 140, Chiraz discloses the method of claim 139, wherein the common image data include texture data (Column 3, line 35).

Prior Art Not Used

Morein et al, U.S. Patent 6,473,086, parallel graphics processors, once the image data for the frame has been generated, the portions generated by each processor can be combined into a single memory structure such that a display driver can easily fetch the color data it requires to generate a display signal.

Response to Arguments

12. The Applicant asserts references Chiraz, U.S. Patent 6,411,302, in view of MacInnis, et al, U.S. Patent 6,573,905, and Bright, et al, U.S. Patent 6,128,025, do not disclose features of claims 1, 110, in that of a single display, one or more merger units operable to synchronously receive frame image from local frame buffer and to synchronously produce a combined image,

no disclosure of plurality of graphics processors able to render frame image data into a local frame buffer (Page 13, 4th Paragraph; Page 14, 1st Paragraph; Page 14, 3rd Paragraph through Page 15, 1st Paragraph; Page 16, 1st Paragraph).

The Examiner respectfully notes, however, that Chiraz discloses a single display (Figure 1, Column 11, lines 9-14; Figure 23A-B, Column 21, lines 39-45; Column 38, lines 40-46) and a plurality of processors (Figure 9, elements 32A, 32N, Column 13, lines 28-32; Figure 25, elements 176, 180, 184, Columns 23-24; Column 16, lines 54-57; *AGP Bus*, Column 13, lines 36; I, Column 16, lines 54-58) able to render to a local frame buffer. Littlefield teaches multiple graphics processors with multiple frame buffers (Figures 1-8, Column 4, line 60-64). MacInnis teaches and one or more merge units operable to synchronously receive the frame image data; from the respective local frame buffers and to synchronously produce combined frame image data based thereon (Column 6, line 17; Figure 4, elements 94, 108; Column 9, lines 25-36). Bright teaches synchronously produce frame image data (Column 2, lines 48-50, 55-58; Column 9, lines 55-60, *each driving a portion of the LCD display*).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Allen E. Quillen whose telephone number is (703) 605-4584. The examiner can normally be reached on Tuesday – Friday, 8:30am – noon and 1:00 - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella, can be reached on (703) 308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or FAX'd to:

(703) 872-9314 (for Technology Center 2600 only)

Hand delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Sixth Floor (Receptionist), Arlington, Virginia

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number (703) 305-9600 or (703) 305-3800.

Allen E. Quillen
Patent Examiner
Art Unit 2676

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February 2, 2004

MATTHEW C. BELLA
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